IME-03-003

Arpil 6, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/767,275 01/29/04 |

Ming Fu Li et al.

CMOS COMPATIBLE LOW BAND OFFSET DOUBLE BARRIER RESONANT TUNNELING DIODE

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 12, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date SBA 4/12/04

L.L. Chang et al., "Resonant tunneling in the semiconductor double barriers," Appl. Phys. Lett., Vol. 24, pp. 593-595, June 1974, demonstrates a resonant tunneling diode consisting of the two potential barriers separated by the well using the III-V compound semiconductor.

J.P. Sun et al., "Resonant Tunneling Diodes: Models and Properties," Proc. of the IEEE, Vol. 86, No. 4, April 1998, pp. 641-661, Semiconductor Industry Association (SIA), The international roadmap for semiconductors 2001, offers the capability of operation of an oscillator, an amplifier and a mixer at extremely high frequency with high resonant current density and a very low noise.

Ikeda et al., "Resonant tunneling characteristics in SiO2/Si double-barrier structures in a wide range of applied voltage," Applied Physics Letters, Vol. 83, No. 7, Aug. 2003, pp. 1456-1458, reports on the SiO2 double barrier structure with silicon well.

Kim et al., "Effect of Barrier Thickness on the Interface and Optical Properties of InGaN/GaN Multiple Quantum Wells," Jpn. J. Appl. Phys., Part 1, 40, 3085 (2001), investigates the effect of barrier thickness on the interfacial and optical properties of the InGaN/GaN multiple quantum wells grown in a low-pressure metalorganic chemical vapor deposition system.

Huang et al., "Sub 50-nm FinFET: PMOS," IEDM 99-67, 3.4.1 to 3.4.4, reports P-channel FinFET results, demonstrating the promise of the FinFET structure as a future CMOS technology.

Wong et al., "Self-Aligned (Top and Bottom) Double-Gate MOSFET with a 25 nm Thick Silicon Channel," 1997 IEDM Technical Digest, pp. 16.6.1 to 16.6.4, reports a fabrication method that attains the "ideal" double-gate MOSFET device structure.

Wilk et al., "High-k gate dielectrics: Current status and materials properties considerations," J. Appl Phys., Vol. 89, No. 10, May 15, 2001, pp. 5243-5275, discusses low band offset materials which are also high-k dielectrics and are being extensively studied and now used as gate dielectrics in the context of other types of solid state devices.

U.S. Patent 6,208,555 to Noble, "Negative Resistance Memory Cell," discusses an SRAM memory cell that includes two tunnel diodes coupled in series and a MOSFET.

U.S. Patent Application Publication US 2003/0049894 A1 to Berger et al., "Si-Based Resonant Interband Tunneling Diodes and Method of Making Interband Tunneling Diodes," discusses interband tunnel diodes which are compatible with Si-based processes.

U.S. Patent 6,512,274 to King et al., "CMOS-P rocess Compatible, Tunable NDR (Negative Differential Resistance) Device and Method of Operating Same," teaches the formation of an n-channel metal-insulator-semiconductor field effect transistor (MISFET), which also exhibits the NDR property.

U.S. Patent 6,528,370 to Suzuki et al., "Semiconductor Device and Method of Manufacturing the Same," teaches the formation of a device that includes a conducting channel layer, a floating region (insulated from the channel) above the channel layer and a quantum well region disposed between the floating region and the channel layer.

The following two U.S. Patents disclose a resonant tunneling diode formed by layering silicon dioxide barrier layers on either side of a germanium well:

1) U.S. Patent 5,466,949 to Okuno, "Silicon Oxide Germanium Resonant Tunneling."

2) U.S. Patent 5,616,515 to Okuno, "Silicon Oxide Germanium Resonant Tunneling."

U.S. Patent 6,239,450 to Harvey et al., "Negative Differential Resistance Device Based on Tunneling Through Microclusters, and Method Therefor" discloses a negative differential resistanace type device formed by inducing the growth of silicon crystalline microclusters within a matrix of amorphous silicon.

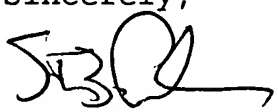
U.S. Patent 5,606,177 to Wallace et al., "Silicon Oxide Resonant Tunneling Diode Structure," discloses a resonant tunnel diode made of a silicon quantum well surrounded by silicon dioxide barrier layers which are perforated to insure crystal alignment.

U.S. Patent 6,208,555 to Noble, "Negative Resistance Memory Cell and Method," discloses a SRAM memory cell including two tunnel diodes coupled in series and a MOS FET.

European Patent Application EP 1 168 456 A2 to King et al., "A CMOS-process compatible, tunable NDR (negative differential resistance) device and method of operating same," discloses an n-channel metal-insulator-semiconductor field-effect transistor (MISFET) that exhibits negative differential resistance in its output characteristic (drian current as a function of drain voltage.

European Patent Application 0 668 618 A2 to Bate et al., "Resonant tunneling devices," discloses Si/CaF2, Al/CaF2 and Al/Si/Al/Si resonant tunneling devices.

Sincerely,



Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
IME-03-009	10/767,275
Applicant: Ming Fu Li et al.	
Filing Date: 01/29/04	Group Art Unit:

U. S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	6208555	3/27/01	Noble	365	159	3/30/99
	6512274	1/28/03	King et al.	257	369	6/22/00
	6528370	3/4/03	Suzuki et al.	438	257	7/29/02
	5466949	11/14/95	Okuno	257	25	8/4/94
	5616515	4/1/97	Okuno	438	478	6/7/95
	6239450	5/29/01	Harvey et al.	257	49	1/14/99
	5606177	2/25/97	Wallace et al.	257	25	12/6/94
	6208555	3/27/01	Noble	365	159	3/30/99

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation YES	Translation NO
EP	1168456A2	1/2/02	European Patent App.	H01L	29/788		
	0668618A2	5/19/94	European Patent App	H01L	29/88		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial	
	L.L. Chang et al., "Resonant tunneling in the semiconductor double barriers," Appl. Phys. Lett., Vol. 24, pp. 593-595, June 1974.
	I.P. Sun et al., "Resonant Tunneling Diodes: Models and Properties," Proc. of the IEEE, Vol. 86, No. 4, April 1998, pp. 641-661, (SIA).
	Ikeda et al., "Resonant tunneling characteristics in SiO_2/Si double barrier structures in a wide range of applied voltage," Appl. Phys. Lett., Vol. 83, No. 7, Aug. 2003, pp. 1456-1458.

EXAMINER: DATE CONSIDERED:

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FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

- Kim et al., "Effect of Barrier Thickness on the Interface and Optical Properties of InGaN/GaN Multiple Quantum Wells", Jpn. J. Appl. Phys., Part 1, 40, 3085 (2001).
- Huang et al., "Sub 50-nm FinFET: PMOS", IEDM 99-67, 3.4.1 to 3.4.4.
- U.S. Patent App. Pub. US 2003/0049894 A1 to Barger et al., Pub. 3/13/03, Filed 8/24/01, US Cl. 438/183.

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- Wong et al., "Self-Aligned (Top and Bottom) Double-Gate MOSFET with a 25 nm Thick Silicon Channel," 1997 IEDM Technical Digest, pp. 16.6.1 to 16.6.4.
- Wilk et al., "High-k gate dielectrics: Current status and materials properties considerations," J. Appl. Phys., Vol. 89, No. 10, May 15, 2001, pp. 5243-5275.

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